Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A method of fabricating a flash memory, comprising the steps of:
providing a substrate having a tunneling dielectric layer, a first conductive layer, a pad oxide layer and a patterned mask layer formed thereon;
removing portions of the pad oxide layer, the first conductive layer, the tunneling dielectric layer and the substrate using the patterned mask layer as an etching mask to form a plurality of first trenches in the substrate;
depositing an insulating material into the first trenches to form a plurality of device isolation structures;
removing a portion of each device isolation structure to form a plurality of second trenches such that the top section of each retained device isolation structure lies between the tunneling dielectric layer and the patterned mask layer;
forming a dielectric layer over the substrate to cover the patterned mask layer and the surface of the second trenches;
filling the second trenches with sacrificial material so as to form sacrificial layers;
removing a portion of the dielectric layer using the sacri-

ficial layers as self-aligned masks;
removing the patterned mask layer to expose the pad oxide layer;
removing the pad oxide layer to expose the first conductive layer;
forming a second conductive layer over the substrate;
removing a portion of the second conductive layer to expose a top section of the sacrificial layers, wherein the second conductive layer and the first conductive layer together form a plurality of floating gates;
removing the sacrificial layer;
forming an inter-gate dielectric layer over the substrate to cover the floating gate;
forming a third conductive layer over the inter-gate dielectric layer to form a plurality of control gates; and
forming a plurality of source/drain regions in the substrate on each side of the control gates.

[c2] 2. The method of claim 1, wherein a material of the sacrificial layer and the dielectric layer have different etching selectivity and a material of the sacrificial layer and that of the second conductive layer have different etching selectivities.

[c3] 3. The method of claim 2, wherein the material of the sacrificial layer comprises silicon oxide.

[c4] 4. The method of claim 2, wherein the material of the dielectric layer comprises silicon nitride.

[c5] 5. The method of claim 1, wherein the step for removing a portion of the second conductive layer to expose the top section of the sacrificial layer comprises performing a chemical-mechanical polishing operation.

[c6] 6. The method of claim 1, wherein the dielectric layer and the patterned mask layer are formed by identical material so that the patterned mask layer is also removed in the process of removing a portion of the dielectric layer.

[c7] 7. The method of claim 1, further comprising a step of removing the dielectric layer after the step of removing the sacrificial layer but before the step of forming the inter-gate dielectric layer.

[c8] 8. The method of claim 1, wherein the step of forming the second trenches comprises etching back in a dry etching operation.

[c9] 9. The method of claim 1, further comprising a step of totally removing the first conductive layer after the step of removing the pad oxide layer but before the step of forming the second conductive layer.

[c10] 10. A method of fabricating a floating gate, comprising the steps of:
providing a substrate having a plurality of device isolation structures for defining an active region and a tunneling oxide layer and a patterned mask layer sequentially formed within the active region over the substrate;
removing a portion of each device isolation structure to form a plurality of trenches, wherein the top section of each retained device isolation structure is disposed between the tunneling dielectric layer and the patterned mask layer;
forming a dielectric layer over the substrate to cover the patterned mask layer and the surface of the trenches;
filling the trenches with sacrificial material so as to form sacrificial layers;
removing a portion of the dielectric layer using the sacrificial layers as a self-aligned mask;
removing the patterned mask layer to expose the tunneling dielectric layer;
forming a first conductive layer over the substrate;
removing a portion of the first conductive layer to expose the top section of the sacrificial layers; and
removing the sacrificial layers.

[c11] 11. The method of claim 10, wherein a material of the sacrificial layer and the dielectric layer have different

etching selectivities and a material of the sacrificial layer and the first conductive layer have different etching selectivities.

[c12] 12. The method of claim 11, wherein the material of the sacrificial layer comprises silicon oxide.

[c13] 13. The method of claim 11, wherein the material of the dielectric layer comprises silicon nitride.

[c14] 14. The method of claim 10, wherein the step for removing a portion of the first conductive layer to expose the top section of the sacrificial layer comprises performing a chemical-mechanical polishing operation.

[c15] 15. The method of claim 10, wherein the dielectric layer and the patterned mask layer are formed by identical material so that the patterned mask layer is also removed in the process of removing a portion of the dielectric layer.

[c16] 16. The method of claim 15, wherein a material of the dielectric layer and the patterned mask layer comprises silicon nitride.

[c17] 17. The method of claim 10, wherein the step of forming the trenches comprises etching back in a dry etching operation.

[c18] 18. The method of claim 10, further comprising a step of removing the dielectric layer after the step of removing the sacrificial layers.

[c19] 19. The method of claim 10, wherein a second conductive layer and a pad oxide layer are formed between the tunneling oxide layer and the patterned mask layer, and the method further comprises a step of removing the pad oxide layer after the step of removing the mask layer.

[c20] 20. The method of claim 19, further comprising a step of removing the second conductive layer after the step of removing the pad oxide layer.